Claims

1. A circuit layout configuration in which a first and a second transistors are composed of a first cell, a second cell, a third cell and a fourth cell, each cell including four sub-transistors, and formed of 16 sub-transistors arrayed in a matrix with four rows and four columns as a whole, and the circuit layout configuration being characterized by that the first cell is structured so that the sub-transistors forming the second transistor are disposed at a first row and a first column and at a second row and a second column and the sub-transistors forming the first transistor are disposed at the first row and the second column and at the second row and the first column and the sub-transistors are disposed symmetrically with respect to a common center, that the second cell is disposed axisymmetrically to the first cell, and that the third cell and the fourth cell are disposed axisymmetrically to the first cell and the second cell.

2. The circuit layout configuration of claim 1, wherein a gate of each of the sub-transistors forming the first transistor and a gate of each of the sub-transistors forming the second transistor are connected in common, and the first transistor and the second transistor form a current mirror circuit.

3. The circuit layout configuration of claim 1, wherein gates of the sub-transistors forming the first transistor are connected in common to form a gate of the first transistor and gates of the sub-transistors forming the second transistor are connected in common to form a gate of the second transistor.

4. The circuit layout configuration of claim 3, wherein the first and second transistors form differential input pair transistors of an operational amplifier.

5. The circuit layout configuration of claim 1, 2, 3 or 4, wherein sources of the sub-transistors forming the first transistor are connected in common and drains of the sub-transistors forming the first transistor are connected in common.

6. The circuit layout configuration of claim 5, wherein sources of the sub-transistors forming the second transistor are connected in common and drains of the sub-transistors forming the second transistor are connected in common.

7. The circuit layout configuration of claim 1, 2, 3 or 4, further comprising a

plurality of circuits, each comprising the first cell, the second cell, the third cell and the fourth cell and disposed axisymmetrically.